| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/877,583 | DIETL ET AL. | |
| | Examiner | Art Unit | |
| | Shuwang Liu | 2634 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 01/10/2005*.

2. ☒ The allowed claim(s) is/are *1 and 2*.

3. ☒ The drawings filed on *08 June 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *04/20/05* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## DETAILED ACTION

## EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with J. Dennis Moore, who proposed the following examiner's amendment, on April 20, 2005.

The application has been amended as follows:

(A) In Specification, the first paragraph (lines 1-22) on page 11 is replaced by the following:

As evident in the starting condition shown, there is a connection between the current sources S1-S32 and the charging circuit L1 via the closed switches PS1a-1 to PS1a-32 and PS1b-2 to PS1b-32 ~~PS1b-2-PS1b-32~~ as well as via the closed separating switches TR1a, TR1a-1 and TR2b to TR32b ~~TR2b-TR32b~~ and TR1b-2 to TR1b-32. When the signal SM1 derived from the phase signal Ph1 attains from the multiplexer 12 the input 20 all switches PS1a-1 to PS1a-32 are opened, prior to which at to the output voltage V1 at the output of the charging circuit L1 was at its lowest value as evident from the plot in FIG. 3. Opening the switches PS1a-1 to PS1a-32 merely parts the current source S1 from the charging circuit L1, the other current sources S2 to S32 continuing

to be connected to the charging circuit L1 via the closed separating switches TR2b to TR32b ~~TR2b-TR32b~~ and TR1b-2 to TR1b-32 ~~TR1b-2-TR1b-32~~ and closed phase switches PS1b-2 to PS1b-32. This is why the output voltage V1 increases only unsubstantially up to the point in time t(1). When then at the point in time t(1) the signal SM2 from multiplexer 14 likewise attains the input 22 prompting changeover of the phase switches PS1b-1 to PS1b-32 into the closed condition then the output voltage V1 increases as plotted in FIG. 3 up to its maximum value with charging of the capacitor C1.

(B) In claims, claims 1 and 2 are replaced by the following claims:

1. A circuit for generating an output phase signal with a variable phase shift relative to a reference phase, including

an oscillator outputting phase signals at n outputs, each of which is shifted in phase by $\varphi = 360°/n$ from one output to the next and is correspondingly staggered in time relative to each other by $\Delta t$,

a first multiplexer, the inputs of which are connected to the even-number outputs of the oscillator and which passes on to its output a phase signal output by an output x of the oscillator as a function of a first phase selection signal output by a phase select circuit, where x is a selected one of the n outputs of the oscillator,

a second multiplexer, the inputs of which are connected to the odd-number outputs of the oscillator and which passes to its output on a phase signal output by an output x + 1 of the oscillator as a function of a second phase selection signal output by the phase select circuit,

a phase interpolator receiving the phase signals output by the multiplexers and controlling with these the periodic opening and closing of a first set of phase switches in the time spacing of $\Delta t$,

the phase interpolator containing a first charging circuit in which a charging voltage of a capacitor is varied by switching current sources assigned to the first set of phase switches on or off in accordance with the closing or opening of the first set of phase switches,

whereby a number of current sources is provided corresponding to the number of interphase shift values to be generated between the phase shifts of the phase signals output by the first and second multiplexers, to each of which at least two phase switches are assigned, of which the one in each case is controlled by the phase signal output by the first multiplexer and the other by the phase signal output by the second multiplexer, a first ~~set of~~ separating switch ~~switches~~ being inserted in the connection between a first ~~each~~ of the at least two phase switches and the assigned current source, an a second separating switch being inserted in the connection between a second of the at least two phase switches, thereby providing a first set and a second set of separating switches for said number of current sources,

characterized in that

in each connection between each of said first phase switches ~~switch~~ and the first charging circuit a third ~~second set of~~ separating switch ~~switches~~ is inserted, and in each connection between each of said second phase switches a fourth set of separating switches is inserted, thereby providing a third set and a fourth set of separating switches,

and that a control circuit ~~(SS1-SS32)~~ is provided for each current source which ensures that the first set and the third set of separating switches ~~(TR1a to TR32a, TR1b to TR32b)~~ assigned to each phase switch operate in a first phase ~~(PS1a-1 to PS1a-32, PS1b-1 to PS1b-32)~~ and the second set and the fourth ~~second~~ set of separating switches ~~(TR1a-1 to TR1a-32, TR1b-1 to TR1b-32)~~ assigned to the same phase switch operate in a second phase reverse to the first phase, and are activated to switch the separating switches for the current sources in a cycling sequence ~~are never open at the~~

~~same time~~ when there is a change in the phasing of the output phase signal ~~output by the circuit~~ relative to the reference phase.

2. The circuit in claim 1, characterized in that a second charging circuit ~~(L2)~~ is provided, that parallel to each of the first phase switches ~~switch~~ a third ~~second~~ set of phase switches ~~(PS2a-1 to PS2a-32, PS2b-1 to PS2b-32)~~ is arranged, and parallel to each of the second phase switches a fourth set of phase switches is arranged, which can be switched opposite in phase to that of the ~~assigned~~ phase switch with which it is in parallel, and that in the connection between the third ~~second~~ phase switch in each case and the second charging circuit a fifth ~~further~~ set of separating switches ~~(TR2a-1 to TR2a-32, TR2b-1 to TR2b-32)~~ is inserted in each case which is signaled equal in phase to the third set ~~first and second sets~~ of separating switches and that in the connection between the fourth phase switch in each case and the second charging circuit a sixth set of separating switches is inserted in each case which is signaled equal in phase to the fourth set of separating switches ~~located between a current source and the first charging circuit (L1)~~, resulting in a second output phase signal (V2) being producible from the second charging circuit (L2) which is phase-shifted by 180° relative to the output phase signal (V1) generated by the first charging circuit (L1).

***Allowable Subject Matter***

2. Claims 1 and 2 are allowed.

3. The following is a statement of reasons for the indication of allowable subject matter: The present invention comprises an oscillator outputting phase signal at n outputs, a first multiplexer, a second multiplexer, and a phase interpolator. The closest

prior art, Masenas et al. (US Patent Number 6,525,615) shows a similar system which also includes an oscillator outputting phase signal at n outputs, a first multiplexer, a second multiplexer, and a phase interpolator (see figure 1). However, Masenas et al. fails to disclose a phase interpolator having charging circuits, a control circuit, separating switches as recited in claims. The distinct features have been added to the independent claim 1, in addition the priority date of the application has earlier date than the filing date the patent application, therefore, rendering them allowable.

***Conclusion***

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shuwang Liu whose telephone number is 571 272-3036. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shuwang Liu
Primary Examiner
Art Unit 2634

April 20, 2005